

CSB6xx Comparison Matrix – for more information, go to www.cogcomp.com

The CSB6xx series boards cover a variety of CPU's and functions. The following table provides a matrix of their features for easy comparison:

	CSB625	CSB626	CSB637	CSB650	CSB655	CSB672
Microprocessor (Core)	Intel PXA255 (XScale)	Intel PXA270 (XScale)	Atmel AT91RM9200 (ARM920T)	AMD Au1100 (Au1/MIPS32)	AMD Au1550 (Au1/MIPS32)	AMCC 405EP (IBM 400)
Core/SDRAM/Bus Clock	400Mhz/100Mhz/50Mhz	524Mhz/100Mhz/50Mhz	184Mhz/92Mhz/92Mhz	392Mhz/98Mhz/49Mhz	492Mhz/266Mhz/66Mhz	266Mhz/133Mhz/66Mhz
I-Cache/ D-Cache	32KB/32KB	32KB/32KB	16KB/16KB	16KB/16KB	16KB/16KB	16KB/16KB
MMU	Yes	Yes	Yes	Yes	Yes	Yes
Internal SRAM	-	256KB	16KB	-	-	4KB
FLASH	8MB (16MB/32MB opt.)	8MB (16MB/32MB opt.)	8MB (16MB opt.)	8MB (16MB/32MB opt.)	8MB (16MB/32MB opt.)	8MB (16MB/32MB opt.)
SDRAM	64MB SDR	64MB SDR (128MB opt.)	64MB SDR (128MB opt.)	64MB SDR (128MB opt.)	64MB DDR (128MB opt.)	64MB SDR (128MB opt.)
1-Wire Silicon ID	DS2401	DS2401	DS2401	DS2401	DS2401	DS2401
Expansion Bus Add/Data	25/16	26/16	24/16	25/16	25/16	26/16
PCI Bus	-	-	-	-	32-Bit PCI, 33/66Mhz	32-Bit PCI, 33/66Mhz
RS232 UARTS	FF UART @ 230Kb (RX/TX Only)	STD UART @ 230Kb (RX/TX Only)	Debug UART @ 115Kb	UART0 @ 230Kb	UART0 @ 230Kb	UART0 @ 230Kb
Additional TTL UARTS (via Expansion Conn.)	STD UART @ 230Kb BT UART @ 921Kb HW UART @ 230kb	FF UART @ 230Kb BT UART @ 921Kb	UART0-3 @ 3.8Mbps	UART1 and 3 @ 1.5Mb (there is no UART2)	UART1 and 3 @ 1.5Mb (there is no UART2)	UART1 @ 4Mbps
IrDA Support	on STD UART @ 4Mb, on FF UART @ 115Kb on HW UART @ 115kb	STD UART @ 4MB (requires disabling of on board RS232 buffer)	on UART0-3 @ 115K	IR UART @ 4Mb	-	-
SPI (via Expansion Conn.)	SSP @ 1.8Mb NSSP @ 13Mb (muxed with HW UART)	SSP 1-3 @ 13Mb	SPI 1 @ 15Mb	SPI 1 @ 25Mb	M SPI 1,2 @ 25Mb (SPI 2 is muxed w/AC'97)	-
I2C (via Expansion Conn.)	Internal 400KBps Controller	Internal 400KBps Controller	Internal 400Kb Controller	Programmed I/O via GPIO	Internal 400KBps via PSC0-2	Internal 400KBps Controller
SD/MMC Interface (via Expansion Conn.)	1-Bit SDIO	4-Bit SDIO	4-Bit SDIO	Dual 4-Bit SDIO	SPI Mode Only	-
USB Device Ports (via Expansion Conn.)	1 Internal, 1 via TD242LP (muxed with one host port)	1 Internal	1 Internal	1 Internal (shared with Host port 0)	1	-
USB Host Ports (via Expansion Conn.)	2 via TD242LP	1 Internal	2 Internal	2 Internal (1 configurable as device)	1 (also configurable as a USB Device Port)	-
USB OTG Support	Yes via TD242LP	Yes	-	-	Yes	-
Ethernet Interface	CS8900a	CS8900a	Internal MAC	Internal MAC	Internal Dual MAC	Internal Dual MAC
On Board PHY	-	-	BCM5221	BCM5221	BCM5222 Dual PHY	BCM5222 Dual Phy
AC'97 Audio	UCB1400 on board	UCB1400 on board	-	UCB1400 on board	Yes via PSC0-2	-
I2S Audio (via GPIO Conn.)	Yes if UCB1400 removed	Yes if UCB1400 removed	Yes via SSI 0 and SSI1	Yes	Yes via PSC3 only	-
PCMCIA/Compact Flash (via Expansion Conn.)	Both (25 Address bits only)	Both	CF Only	Both (25 Address bits only)	Both (25 Address bits only)	-
LCD I/F, Max Resolution and Depth	Internal 640x480, 16Bpp	Internal 640x480, 16Bpp	S1D13506 800x600, 16Bpp	Internal 800x600, 16Bpp (HW Rotate up to QVGA)	-	-

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Touch Interface	4-Wire via UCB1400	4-Wire via UCB1400	None	4-Wire via UCB1400	-	-
Dedicated PWM	2	4	4 via Internal Timers.	2	-	-
JTAG Debug	Yes	Yes	Yes	Yes	Yes	Yes
Embedded Trace	-	-	Yes	-	-	Yes
Dedicated Battery Input for RTC	-	Yes	-	-	Yes	-
Battery Charger	BQ24105 2 Cell (3 opt.) Lithium Ion charger, 2 Amp Charge Current	BQ24105 2 Cell (3 opt.) Lithium Ion charger, 2 Amp Charge Current	-	BQ24105 2 Cell (3 opt.) Lithium Ion charger, 2 Amp Charge Current	-	-
Available GPIO (no LCD) (no Audio) (no CF)	9 (+20) (+5) (+10)	40 (+20) (+5) (+10)	20 (+0) (+5) (+0)	8 (+0) (+0) (+5)	8 (+0) (+0) (+5)	26 (+0) (+0) (+0)
Other Features	-	SIM Card I/F, Matrix Keypad I/F, CMOS Camera I/F and Smart LCD I/F	-	SDRAM has it's own Address and Data bus @ 98Mhz (SDR)	SDRAM has it's own Address and Data bus @ 266Mhz (DDR)	SDRAM has it's own Address and Data bus @ 133Mhz (SDR)
Input Voltage	6V to 20V (25V w/o Battery Charger)	6V to 20V (25V w/o Battery Charger)	6V to 35V	6V to 20V (25V w/o Battery Charger)	6V to 35V	6V to 35V
3.3V Power to Target	3.3V @ 3A	3.3V @ 3A	3.3V @ 3A	3.3V @ 3A	3.3V @ 3A	3.3V @ 3A
Board Dimensions	44.5mm x 63.5mm x 0.9mm (1.75" x 2.5" x 0.35")	44.5mm x 63.5mm x 0.9mm (1.75" x 2.5" x 0.35")	44.5mm x 63.5mm x 0.9mm (1.75" x 2.5" x 0.35")	44.5mm x 63.5mm x 0.9mm (1.75" x 2.5" x 0.35")	44.5mm x 63.5mm x 0.9mm (1.75" x 2.5" x 0.35")	44.5mm x 63.5mm x 0.9mm (1.75" x 2.5" x 0.35")

Table Notes:

1. KB = 1024 bytes, MB = 1,048,576 bytes, Kb = Kilobits/sec, Mb = Megabytes/sec.
2. Default programmed clock rate of the CSB6xx Expansion Address/Data Bus is 66Mhz or less. The SDRAM speed is limited to this clock rate for devices that share the same Address/Data bus with the SDRAM. Faster operation may be possible depending upon the target interface, but is not guaranteed. Actual board clock rate is also dependant upon the internal clocks from which the SDRAM and Address/Data Timing is derived.
3. RS232 UART Baud rates are manufacturers stated maximum baud rate if less than the maximum baud rate supported by the RS232 Transceivers (230Kbps). TTL UART Baud rates are the manufacturers stated maximum baud rate. For any UART, the actual achievable baud rate may be lower.
4. SPI ports are limited by the manufacturers maximum recommended clock rates, or by the speed of the slave devices on the users target board.
5. Stated LCD Resolution is the maximum supported by that controller, however, internal LCD Controllers may be limited to lower resolutions and/or color depths based on available bandwidth.
6. "via Expansion Conn." indicates the signals are made available on one of the Expansion Connectors.
7. The number of GPIO represents the minimum available with the LCD, Audio and Compact Flash interfaces all being used. The next 3 rows show the additional GPIO that would be available when the respective function is not used. There is no increase if the board does not have that function to disable (such AC'97 or Compact Flash). Many GPIO share the pins with internal peripheral functions and use of these peripheral functions will reduce the number GPIO available correspondingly.